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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,772	08/01/2005	Christopher Rodd Speirs	CH02 0021 US	4888

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NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
ABDIN, SHAHEDA A	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
07/27/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/518,772	SPEIRS ET AL.	
	Examiner	Art Unit	
	Shaheda A. Abdin	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Abstract of the discloser is objected to because the abstract is exceeded more than 150 words. Appropriate correction is required.

4. Page 5, lines 21-25 of the specification recites the phrases "as claimed in claims 1 to 8" and " as claimed in claim 9" should be deleted because claims 1 to 9 may be canceled or amended.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Objections

5. Claims 1-12 are objected to because of the following informalities: The use of parentheses in claims 1-12 are improper because the parentheses uses only for the reference characters (see MPEP 608.O1(M)). Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1,6 -7,10,11-12 are rejected under 35 U.S.C. 102(b) as being anticipated by He et al. (US. Patent No: 6323849 B1).

(1) Regarding claim1:

He teaches a circuit arrangement for controlling a display device (150) which can be operated in a partial mode (column 1, lines 53-61) , comprising a row drive circuit (140) for driving n rows (141-149) of the display device (150) and a column drive circuit (130) for driving m (131-139) columns of the display device, wherein the row drive circuit (140) controls the n rows (141-149) of the display device sequentially from 1 to n (141-149), and the column drive circuit (130) supplies column voltages to the m columns (131-139), which voltages correspond to the picture data to be displayed of pixels of the controlled row, logic function (220-230, see fig. 2) is included in the row drive circuit 140 in front of at least one row (141-149) to which logic function a first control signal (105) can be supplied, said first control signal (105) achieving a

deactivation/activation (a fraction of display that can be turn off by the controller 110 which is connected to the row driver 140 turn, see column 3, lines 3-7) of the row output (out put to the row lines 141-149) in dependence on the partial mode (partial display mode activating area) (column 2, lines 41-46, column 3, lines 1-30, fig. 1 and 2).

(2) Regarding claim 6:

He teaches that a control logic (220-230, see fig. 2) in the column drive circuit (130) generates the first control signal (105) in dependence on a partial mode and supplies it to the row drive circuit (130) (column 2, lines 41-46, column 3, lines 1-30, fig. 1).

(3) Regarding claim 7:

He teaches that the column drive circuit (130) supplies no column voltages to the column outputs (output to the data line 131 -139) in the case of a line that is not to be displayed (when the full display is active, both control lines 111, 118 are pulled low (logic zero). Using AND logic gates 220, 230 connected using lines 225, 235 to the inputs of an XOR logic gate 240, a reset signal is created on reset line 113 based on the number of lines that have already been activated and the partial display control signals; note that display portion or lines are controlled by a driving column voltage when the display portion is showing by lines in the display and driving in a manner that if there is no column voltage in certain lines, no display is available in that lines because pixel in a row occurred when voltage is applied to that pixel ; which means no column voltage is driving to the line in the case of a line that not to be displayed (also see column (column 3, lines 12-30).

(4) Regarding claim 10:

He teaches that a display device (150) comprising a circuit arrangement (column 2, lines 41-46, column 3, lines 1-30 and Fig. 1 - 2).

(5) Regarding claim 11:

He teaches an electronic appliance (circuit) splay device (150) (column 2, lines 41-46, fig 2-4).

(6) Regarding claim 12:

Note the discussion of He above in claim 1 which is similar to claim 12.Only the different, claim 1 is an apparatus and claim 12 is a method claim.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2-3, 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over He et al. (US Patent No: 6323849 B1) in view of Janssen et al. (US Pub: 20030025665 A1).

(1) Regarding claim 2:

Note the discussion of he above. He discloses the logic function but did not discloses that logic function is connected in front of each row output.

However, Janssen in the same field of endeavor discloses that the logic function (28, 29) is connected in front of each row (row n, row k) output ([0019], Fig.1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate logic functions (28,29) as taught by Janssen into the row driver of He so that logic function can be connected in front of each row output of the row driver circuit. In this configuration the system will have faster response time with reduced voltage-dependent capacitance ([0008], Janssen).

(2) Regarding claim 3:

Janssen teaches that the logic function (28,29) is realized as an AND Gate ([0019]).

(5) Regarding claim 5:

He teaches that the second control signal (113) is capable of switching (reset from 'on' state to 'off' state) off all n row outputs (cleared of data) by means of the logic functions (220, 2300) during the control (control by the control circuit 110) of a line that is not to be displayed in the partial mode (note that When the full display is active, both control lines 111, 118 are pulled low (logic zero). Using AND logic gates 220, 230 connected using lines 225, 235 to the inputs of an XOR logic gate 240, a reset signal is created on reset line 113 (control by 110) based on the number of lines that have already been activated and the partial display control signals (i.e, screen has partial data) When the reset line 113 goes low, the shift registers of the column drivers 130, shown in FIG. 1 are cleared of data. By resetting the row and column drivers before the full display has been activated (column 3, lines 12-30).

(6) Regarding claim 9:

Note the part of discussion of He above in claim 1 which is similar to claim 9 except the limitation a logic function connected in front of each row output.

However, Janssen in the same field of endeavor discloses that the logic function (28, 29) is connected in front of each row (row n, row k) output ([0019], Fig.1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate logic functions (28,29) as taught by Janssen into the row driver of He so that logic function can be connected in front of each row output of the row driver circuit. In this configuration the system will have faster response time with reduced voltage-dependent capacitance ([0008], Janssen).

10. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over He et al. (US Patent No: 6323849 B1) inview of Sarrasin et al. (US Patent No:5600343).

(1) Regarding claim 4:

Note the discussion of He above. He teaches that the row driver circuit (140) compromise a shift register (column 3 lines 43-45) , but He does not teaches that the shift register has n stages and n outputs, and in that a second control signal can be supplied to the shift register at the input thereof for controlling the consecutive rows 1 to n, which second control signal activates the outputs of the shift register consecutively in dependence on a clock signal.

However, Sarrasin in the same field of endeavor discloses the shift register (30) has n stages (32_1-$32i$) and n outputs (output at (34_1-34) and in that a second control signal (D) can be supplied to the shift register at the input (input data signal) thereof for controlling the consecutive rows (L1-Li), which second control signal

activates the outputs (output at (34_1-34) of the shift register (30) consecutively in dependence on a clock signal (Cp) (column 5, lines 43-67, fig. 3).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to incorporate the shift register (30) which has n stages (32_1-$32i$) and n outputs (output at (34_1-34) and in that a second control signal (D) can be supplied to the shift register at the input (input data signal) as taught by Sarrasin so that for controlling the consecutive rows, which second control signal activates the outputs of the shift register consecutively in dependence on a clock signal . In this configuration the system would be provided a significant reduction of the electrical consumption as a function of the image to be displayed (Sararsin, column 3, lines 61-63).

(2) Regarding claim 8:

Sarrasin teaches that the frequency of the clock signal (Cp) can be increased in the case of one or several consecutive rows (unused rows) that is or are not to be displayed (note that for each rising of the clock Cp the position of logic level '1' is on D then a logic '0' for all following clock stork. It should be noted that '0' is corresponds to the unselected rows, therefore, frequency of the signal will be increased in a manner that frequency of the clock Cp can be increased when the respective row line is turning off for the deactivateor partial turning off position (see column 6, lines 17-35).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's discloser. Yatabe (US PU. No: 6633287) discloses a power supply circuit of an electro-optical device and a method of driving an electro-optical device .

Inquiry

12. Any inquiry concerning this communication should be directed to the examiner at (571) 270-1673 Monday- Friday 7:30 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chanh Nguyen, can be reached at (571) 272-7772.

Information regarding the status on an application may be obtained from the Patent Application information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (tool-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9799 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of patents and trademarks

Washington, D.C. 20231

Or fax to:

(703)872-9314 (for Technology Center 2600 only)

Shaheda Abdin

07/19/2007

CHANH D. NGUYEN
SUPERVISORY PATENT EXAMINER